WE CLAIM:

1. A system for hardening an asynchronous combinational logic circuit against transient faults, comprising in combination:

a first asynchronous register for receiving inputs to be provided to the asynchronous combinational logic circuit, wherein outputs of the first asynchronous register are connected to inputs of the asynchronous combinational logic circuit;

a second asynchronous register for receiving outputs from the asynchronous combinational logic circuit;

a timer operable to ensure data has had sufficient time to propagate through the asynchronous combinational logic circuit; and

a fault detector connected to the outputs of the asynchronous combinational logic circuit, wherein the fault detector is operable to detect a transient fault, and wherein the fault detector resets the asynchronous combinational logic circuit if the transient fault is detected.

2. The system of Claim 1, wherein the asynchronous combinational logic circuit is a null convention logic circuit.

3. The system of Claim 1, wherein the transient fault is a single event upset.

4. The system of Claim 1, wherein the first asynchronous register and the second asynchronous register include at least one null convention logic gate.

5. The system of Claim 1, wherein the timer includes at least one chain of null convention logic gates.

6. The system of Claim 5, wherein the at least one chain of null convention logic gates includes at least as many null convention logic gates as found in a longest path of null convention logic gates in the asynchronous combinational logic circuit.

7. The system of claim 5, wherein the timer includes at least one null convention logic gate operable to create a propagation delay from input to output such that the propagation delay of the timer is at least equal to the longest propagation delay through the asynchronous combinational logic circuit.

8. The system of claim 5, wherein the timer includes at least one resettable null convention logic gate.

9. The system of Claim 5, wherein the timer further includes a fault detector and an inverter, wherein an output of the fault detector provides an input to the inverter.

10. The system of Claim 1, wherein the timer is a long path in pre-existing circuitry.

11. The system of Claim 10, wherein the pre-existing circuitry is the asynchronous combinational logic circuit

12. The system of Claim 1, wherein the fault detector includes a first NAND gate, a second NAND gate, a third NAND gate, a first null convention logic gate, a second null convention logic gate, and an inverter.

13. The system of Claim 12, wherein an output of the first NAND gate and an output of the second NAND gate provide inputs to the third NAND gate, and wherein an output of the third NAND gate provides a fault signal.

14. The system of Claim 13, wherein the fault signal provides a first input to the first null convention logic gate, and wherein the fault signal causes an output of the first null convention logic gate to transition to a logic-1 DATA state if a fault is detected.

15. The system of Claim 12, wherein an output of the second null convention logic gate provides a second input to the first null convention logic gate, and wherein the first null convention logic gate transitions to a logic-0 NULL state when all inputs to the fault detector have transitioned to the logic-0 NULL state.

16. The system of Claim 12, wherein an output of the first null convention logic gate

provides an input to the inverter, and wherein the inverter inverts a fault signal provided by the first null convention logic gate to create an active low Reset to NULL (RSTTN#) signal.

17. The system of Claim 1, wherein the fault detector is a mutual exclusivity fault detector.

18. The system of Claim 1, wherein the fault detector provides as an output a Reset to NULL (RSTTN#) signal.

19. The system of Claim 18, wherein the RSTTN# signal causes a NULL wave front to propagate through the asynchronous combinational logic circuit clearing the transient fault.

20. The system of Claim 18, wherein the RSTTN# signal causes data to be preserved in the first asynchronous register.

21. The system of Claim 20, wherein the asynchronous combinational logic circuit reevaluates itself using the data preserved in the first asynchronous register.

22. A system for hardening a null convention logic circuit against single event upset, comprising in combination:

a first asynchronous register for receiving inputs to be provided to the null convention logic circuit, wherein outputs of the first asynchronous register are connected to inputs of the null convention logic circuit, and wherein the first asynchronous register includes at least one null convention logic gate;

a second asynchronous register for receiving outputs from the null convention logic circuit, and wherein the second asynchronous register includes at least one null convention logic gate;

a timer operable to ensure data has had sufficient time to propagate through the null convention logic circuit, wherein the timer includes at least one chain of null convention logic gates, wherein the at least one chain of null convention logic gates includes at least as many null convention logic gates as found in a longest path of null convention logic gates in the null convention logic circuit, wherein the timer further includes a fault detector and an inverter, and wherein an output of the fault detector provides an input to the inverter; and

a mutual exclusivity fault detector connected to the outputs of the null convention logic circuit, wherein the mutual exclusivity fault detector is operable to detect a single event upset, wherein the mutual exclusivity fault detector resets the null convention logic circuit if the single event upset is detected, wherein the mutual exclusivity fault detector includes a first NAND gate, a second NAND gate, a third NAND gate, a first null convention logic gate, a second null convention logic gate, and an inverter, wherein an output of the first NAND gate and an output of the second NAND gate provide inputs to the third NAND gate, wherein an output of the third

NAND gate provides a fault signal as a first input to the first null convention logic gate, wherein the fault signal causes an output of the first null convention logic gate to transition to a logic-1 DATA state if a fault is detected, wherein an output of the second null convention logic gate provides a second input to the first null convention logic gate, wherein the first null convention logic gate transitions to a logic-0 NULL state when all inputs to the fault detector have transitioned to the logic-0 NULL state, wherein an output of the first null convention logic gate provides an input to the inverter, and wherein the inverter inverts a fault signal provided by the first null convention logic gate to create an active low Reset to NULL (RSTTN#) signal.

23. The system of Claim 22, wherein the RSTTN# signal causes a NULL wave front to propagate through the null convention logic circuit clearing the single event upset.

24. The system of Claim 22, wherein the RSTTN# signal causes data to be preserved in the first asynchronous register.

25. The system of Claim 24, wherein the null convention logic circuit reevaluates itself using the data preserved in the first asynchronous register.

26. A method for hardening an asynchronous combinational logic circuit against transient faults, comprising in combination:

detecting a transient fault;

preserving data in a first asynchronous register;

preventing an output of the asynchronous combinational logic circuit from propagating into a second asynchronous register;

propagating a NULL wave front through the asynchronous combinational logic circuit; and

reevaluating the asynchronous combinational logic circuit using the data preserved in the first asynchronous register.

27. The method of Claim 26, wherein the transient fault is a single event upset.

28. The method of Claim 26, wherein detecting a transient fault comprises connecting a fault detector to the output of the asynchronous combinational logic circuit.

29. The method of Claim 28, wherein the fault detector includes a first NAND gate, a second NAND gate, a third NAND gate, a first null convention logic gate, a second null convention logic gate, and an inverter.

30. The method of Claim 29, wherein an output of the first NAND gate and an output of the second NAND gate provide inputs to the third NAND gate, and wherein an output of the third NAND gate provides a fault signal.

31. The method of Claim 30, wherein the fault signal provides a first input to the first

null convention logic gate, and wherein the fault signal causes an output of the first null convention logic gate to transition to a logic-1 DATA state if a fault is detected.

32. The method of Claim 29, wherein an output of the second null convention logic gate provides a second input to the first null convention logic gate, and wherein the first null convention logic gate transitions to a logic-0 NULL state when all inputs to the fault detector have transitioned to the logic-0 NULL state.

33. The method of Claim 29, wherein an output of the first null convention logic gate provides an input to the inverter, and wherein the inverter inverts a fault signal provided by the first null convention logic gate to create an active low Reset to NULL (RSTTN#) signal.

34. The method of Claim 24, wherein the fault detector is a mutual exclusivity fault detector.

35. The method of Claim 26, wherein preserving data in the first asynchronous register comprises disabling a data acknowledge control signal.

36. The method of Claim 26, wherein the first and second asynchronous registers include at least one null convention logic gate.

37. The method of Claim 26, wherein preventing the output of the asynchronous combinational logic circuit from propagating into the second asynchronous register comprises preventing data from entering the second asynchronous register until the data has enough time to propagate through the asynchronous combinational logic circuit and no transient fault is detected.

38. The method of Claim 26, wherein propagating a NULL wave front results in outputs of the asynchronous combinational logic circuit transitioning to a logic-0 level.

39. The method of Claim 26, wherein reevaluating the asynchronous combinational logic circuit comprises propagating the data in the first asynchronous register to outputs of the asynchronous combinational logic circuit.

40. The method of Claim 26, wherein the asynchronous combinational logic circuit is a null convention logic circuit.